Code: 9F00203

MCA II Semester Supplementary February 2014 Examinations

COMPUTER ORGANIZATION

(For 2009, 2010, 2011 & 2012 admitted batches only)

Time: 3 hours Max. Marks: 60

Answer any FIVE questions
All questions carry equal marks
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1 (a) Perform the arithmetic operations (+70) + (+80) and (-70) + (-80) in binary using signed-2's complement representation for negative numbers.
(b) Simplify the Boolean function F together with the don't care conditions d in
(i) Sum-of-products form and
(ii) Product-of-sums forms
F(w, x, y, z)= $\sum(0, 1, 2, 3, 7, 8, 10)$
d(w, x, y, z)= $\sum(5, 6, 11, 15)$.

2 (a) Draw the block diagram of a typical RAM chip. With the help of a function table explain the operation of the RAM chip.
(b) With the help of a neat diagram, explain the match logic for one word of associative memory.

3 (a) Discuss the organization of the control unit to allow conditional branching in the micro program.
(b) List the advantages and disadvantages of hardwired and micro programmed control.

4 (a) Discuss various addressing modes of 8086 with suitable examples.
(b) List and explain the steps involved in the execution of a complete instruction.

5 (a) Describe the purpose of the following instructions.
(i) AAA.
(ii) CWD.
(iii) RCL.
(b) List and explain the shift and rotate instructions in 8086 microprocessor.

6 (a) Differentiate between the I/O program-controlled transfer and DMA transfer.
(b) With the help of a flowchart explain the sequence of operations carried out during the CPU-IOP communication.

7 (a) What are the difficulties that cause the instruction pipeline to deviate from its normal operation? Explain.
(b) What is an array processor? Explain the two types of array processors.

8 (a) Describe the characteristics of multiprocessors.
(b) Give notes on the following.
(i) Cache coherence.
(ii) Daisy-chain bus arbitration.

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